



SPECIFICATION AMENDMENTS

Please amend the Specification as follows.

[0010] Figures 2a, 2b, 2c, and 2d depict [[is a]] cross-section views of a structure fabricated according to an embodiment of the present invention;

[0012] Figures 4a, 4b, and 4c depict [[is a]] cross-section views of a structure fabricated according to an alternative embodiment of the present invention; and

[0014] Figure 1 is a flowchart illustrating a process 100 for fabricating one or more structures according to an embodiment of the present invention. Figures 2a, 2b, 2c, and 2d depict [[is a]] cross-section views of stages of fabrication of a semiconductor structure 200 using the process 100 according to an embodiment of the present invention. A machine-accessible medium with machine-readable instructions thereon may be used to cause a machine to perform the process 100. Of course, the process 100 is only an example process and other processes may be used to implement embodiments of the present invention.

[0031] Figure 3 is a flowchart illustrating a process 300 for fabricating one or more structures according to an embodiment of the present invention. Figures 4a, 4b, and 4c depict [[is a]] cross-section views of stages of fabrication of a semiconductor structure 400 using the process 300 according to an embodiment of the present invention. A machine-accessible medium with machine-readable instructions thereon may be used to cause a machine to perform the process 300. Of course, the process 300 is only an example process and other processes may be used to implement embodiments of the present invention.

[0033] In a block 302, a layer of material 402 is formed on a wafer 404. The layer 402 may have variations in its surface topology comprising thick [[406]] 411 and thin 408 regions

corresponding to wafer 204 thick 410 and thin 412 regions caused by variations in the surface topology of the wafer 404.

[0034] In a block 304, a sacrificial layer 406 of material is formed on layer 402. The sacrificial layer 406 may have thick 414 and thin 416 regions corresponding to thick and thin regions 410 and 412 of the wafer 404 and/or thick and thin regions [[406]] 411 and 408 of the layer 402.

[0039] In one embodiment, example thick and thin regions 410 and 412 of the wafer 404 may be determined and the narrow and wide regions the narrow and wide regions 428 and 430 of the layer 406 subsequently formed using a zone-compensation technique similar to that described with respect to Figures 1 and 4a through 4c above.

[0042] Example thick and thin regions 410 and 412 of the wafer 404 or the layer 402 may be characterized using a zone-compensation technique (e.g., in-line thickness metrology, frequency yield maps, ellipsometric mapping, laser mapping, capacitance mapping, etc.) similar to that described with respect to Figures 1 and 4a through 4c above. After reading the description herein, a person of ordinary skill will readily recognize how to implement the mapped-compensation technique to form the narrow and wide regions 428 and 430.

DRAWING AMENDMENTS

The attached two sheets of drawings include changes to Figures 2 and 4. These sheets replace the original sheets. Figure 2 has been renumbered Figures 2a through 2d. Figure 4 has been renumbered Figures 4a through 4c. Reference number 406 that represents the thin area in the sacrificial layer 406 has be renumbered 411.

Attachment: Replacement Sheets
Annotated Sheets Showing Changes